

Code No: 117CZ**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD****B. Tech IV Year I Semester Examinations, July/August - 2023****EMBEDDED SYSTEM DESIGN****(Electronics and Communication Engineering)****Time: 3 Hours****Max.Marks:75****Note:** i) Question paper consists of Part A, Part B.

ii) Part A is compulsory, which carries 25 marks. In Part A, answer all questions.

iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART – A**(25 Marks)**

- | | | |
|------|--|-----|
| 1.a) | Give some examples of large-scale embedded systems. | [2] |
| b) | List some applications of embedded systems. | [3] |
| c) | What is a sensor? | [2] |
| d) | What is a relay? What are the different types of relays available? | [3] |
| e) | What is embedded firmware? | [2] |
| f) | What is an absolute object file? | [3] |
| g) | What is process life cycle? | [2] |
| h) | What are the advantages of using user level threads? | [3] |
| i) | What is mutex? | [2] |
| j) | What are the merits and demerits of the priority ceiling? | [3] |

PART – B**(50 Marks)**

- | | | |
|-----------|---|-------|
| 2. | Explain the difference between general computing and embedded systems. | [10] |
| OR | | |
| 3. | Discuss the operational quality attributes that must be addressed in any embedded system development. | [10] |
| 4.a) | Compare general purpose and domain specific processors. | |
| b) | Write a short note on memory shadowing concepts. | [5+5] |
| OR | | |
| 5. | Explain the different types of external communication interfaces in embedded systems. | [10] |
| 6. | What is the role of the reset circuit and watchdog timer in embedded system design? Explain. | [10] |
| OR | | |
| 7. | Explain the high-level language based embedded firmware development technique. | [10] |
| 8. | Explain the different queues associated with process scheduling. | [10] |
| OR | | |
| 9. | Compare the multi-processing and multitasking with suitable examples. | [10] |
| 10. | Explain the shared memory based inter process communication. | [10] |
| OR | | |
| 11. | Explain the architecture of device drivers. | [10] |